

What is claimed is:

1 1. A motherboard in a computing system, wherein said motherboard  
2 comprises:

3 a circuit board including a main voltage plane segment and a separate  
4 voltage plane segment;

5 a microprocessor;

6 a port connector including a connection-sensing terminal;

7 switching means for selectively connecting said main voltage plane  
8 segment to said separate voltage plane segment, wherein said switching means  
9 connects said main voltage plane segment to said separate voltage plane  
10 segment in response to a determination that said connection-sensing terminal is  
11 externally grounded, and wherein switching means disconnects said main  
12 voltage plane segment from said separate voltage plane segment in response to  
13 a determination that said connection-sensing terminal is electrically floating; and

14 a device interface circuit conditioning signals transmitted between said  
15 microprocessor and said port connector, wherein said device interface circuit  
16 draws electrical power from said separate voltage plane segment.

1 2. The motherboard of claim 1, wherein

2 said switching means includes a biasing resistor and a switching device,

3 said switching device has a control terminal connected to said connection-  
4 sensing terminal and connected to a biasing voltage through said biasing  
5 resistor, an input terminal connected to said main voltage plane segment, and an  
6 output terminal connected to said separate voltage plane segment,

7 said input terminal is connected to said output terminal in response to an  
8 application of electrical ground to said control terminal, and

9 said input terminal is disconnected from said output terminal in response  
10 to an application of said biasing voltage to said control terminal.

1 3. The motherboard of claim 2, wherein  
2 said switching device includes a field effect transistor,  
3 said control terminal includes a gate of said field effect transistor,  
4 said input terminal includes a source of said field effect transistor, and  
5 said output terminal includes a sink of said field effect transistor.

1 4. The motherboard of claim 2, wherein said biasing resistor is connected to  
2 said biasing voltage at said main voltage plane.

1 5. The motherboard of claim 1, wherein  
2 said motherboard additionally comprises non-volatile storage,  
3 said switching means includes a biasing resistor, first and second  
4 registers, a switching device, and a switching routine stored within said non-  
5 volatile storage for execution within said microprocessor,

6 said first register includes an input terminal connected to said connection-  
7 sensing terminal and connected to a biasing voltage through said biasing  
8 resistor,

9 said first register is driven to a first state by an application of electrical  
10 ground to said input terminal and to a second state by an application of said  
11 biasing voltage to said input terminal,

12 said switching routine executing within said microprocessor drives said  
13 second register into a third state in response to a determination that said first  
14 register is in said first state,

15 said switching routine executing within said microprocessor drives said  
16 second register into a fourth state in response to a determination that said first  
17 register is in said second state,

18 said switching device has a control terminal connected to an output of  
19 said second register, an input terminal connected to said main voltage plane  
20 segment, and an output terminal connected to said separate voltage plane  
21 segment,

22           said input terminal is connected to said output terminal in response to a  
23 signal applied to said control terminal from said output of said second register  
24 when said second register is in said third state, and

25           said input terminal is disconnected from said output terminal in response  
26 to a signal applied to said control terminal from said output of said second  
27 register when said second register is in said fourth state.

1       6.     The motherboard of claim 5, wherein

2           said switching device includes a field effect transistor,  
3           said control terminal includes a gate of said field effect transistor,  
4           said input terminal includes a source of said field effect transistor, and  
5           said output terminal includes a sink of said field effect transistor.

1       7.     The motherboard of claim 5, wherein said biasing resistor is connected to  
2 said biasing voltage at said main voltage plane.

1       8.     The motherboard of claim 5, wherein said switching routine executing within  
2 said microprocessor periodically examines a state of said first register in  
3 response to clock pulses.

1       9.     The motherboard of claim 5, wherein said switching routine executing within  
2 said microprocessor additionally causes a device driver routine used to condition  
3 signals transferred through said port connector to be loaded in response to a  
4 determination that said first register is in said first state and that said second  
5 register is in said third state.

1       10.    The motherboard of claim 5, wherein said switching routine executing within  
2 said microprocessor additionally causes a device driver routine used to condition  
3 signals transferred through said port connector to be unloaded in response to a

determination that said first register is in said second state and that said second register is in said fourth state.

11. The motherboard of claim 5, wherein

said non-volatile storage additionally holds a system pausing subroutine for execution within said microprocessor in response to an attempt to write or read data through said port connector,

said system pausing subroutine causes a message to be displayed indicating a cable is disconnected and provides a graphical user interface for selecting a retry after said cable is connected, in response to a determination that said second register is in said fourth state, and

said system pausing subroutine causes said attempt to write or read data through said port connector to be retried in response to receiving a selection of said retry from said graphical user interface.

12. A motherboard in a computing system, wherein said motherboard comprises:

a circuit board including a main voltage plane segment;

a microprocessor; and

a plurality of connection subsystems, wherein each connection system within said plurality of connection subsystems includes:

a separate voltage plane segment within said circuit board;

a port connector including a connection-sensing terminal;

switching means for selectively connecting said main voltage plane segment to said separate voltage plane segment, wherein said switching means connects said main voltage plane segment to said separate voltage plane segment in response to a determination that said connection-sensing terminal is externally grounded, and wherein switching means disconnects said main voltage plane segment from said separate voltage plane segment in response to a determination that said connection-sensing terminal is electrically floating; and

16 a device interface circuit conditioning signals transmitted between  
17 said microprocessor and said port connector, wherein said device  
18 interface circuit draws electrical power from said separate voltage plane  
19 segment.

1 13. The motherboard of claim 12, wherein, within each said connection  
2 subsystem,

3 said switching means includes a biasing resistor and a switching device,  
4 said switching device has a control terminal connected to said connection-  
5 sensing terminal and connected to a biasing voltage through said biasing  
6 resistor, an input terminal connected to said main voltage plane segment, and an  
7 output terminal connected to said separate voltage plane segment,

8 said input terminal is connected to said output terminal in response to an  
9 application of electrical ground to said control terminal, and

10 said input terminal is disconnected from said output terminal in response  
11 to an application of said biasing voltage to said control terminal.

1 14. The motherboard of claim 12,

2 wherein said motherboard additionally comprises first and second  
3 registers and non-volatile storage storing a switching routine for execution within  
4 said microprocessor,

5 wherein, within each said connection subsystem,

6 said switching means includes a biasing resistor, bit positions  
7 within said first and second registers, and a switching device,

8 said bit position within said first register includes an input terminal  
9 connected to said connection-sensing terminal and connected to a biasing  
10 voltage through said biasing resistor, and

11 said bit position within said first register is driven to a first state by  
12 an application of electrical ground to said input terminal and to a second  
13 state by an application of said biasing voltage to said input terminal,

14                   said switching routine executing within said microprocessor drives  
15                   said bit position within said second register into a third state in response  
16                   to a determination that bit position of said first register is in said first state,  
17                   said switching routine executing within said microprocessor drives  
18                   said second register into a fourth state in response to a determination that  
19                   said bit position in said first register is in said second state, and  
20                   wherein, within each said connection subsystem,  
21                   said switching device has a control terminal connected to an output  
22                   of said second register, an input terminal connected to said main voltage  
23                   plane segment, and an output terminal connected to said separate  
24                   voltage plane segment,  
25                   said input terminal is connected to said output terminal in response  
26                   to a signal applied to said control terminal from said output of said second  
27                   register when said second register is in said third state, and  
28                   said input terminal is disconnected from said output terminal in  
29                   response to a signal applied to said control terminal from said output of  
30                   said second register when said second register is in said fourth state.

1           15. The motherboard of claim 14, wherein for each said connection  
2           subsystem, said switching routine executing within said microprocessor  
3           additionally causes a device driver routine used to condition signals transferred  
4           through said port connector to be loaded in response to a determination that said  
5           first register is in said first state and that said second register is in said third  
6           state.

1           16. The motherboard of claim 14, wherein for each said connection  
2           subsystem, said switching routine executing within said microprocessor  
3           additionally causes a device driver routine used to condition signals transferred  
4           through said port connector to be unloaded in response to a determination that

5 said first register is in said second state and that said second register is in said  
6 fourth state.

1 17. The motherboard of claim 14, wherein

2 said non-volatile storage additionally holds a system pausing subroutine  
3 for execution within said microprocessor in response to an attempt to write or  
4 read data through a port connector within a connection subsystem in said  
5 plurality of connection subsystems,

6 said system pausing subroutine causes a message to be displayed  
7 indicating an external cable to said port connector is disconnected and provides  
8 a graphical user interface for selecting a retry after said external cable is  
9 connected, in response to a determination that said second register within said  
10 connection subsystem is in said fourth state, and

11 said system pausing subroutine causes said attempt to write or read data  
12 through said port connector to be retried in response to receiving a selection of  
13 said retry from said graphical user interface.

1 18. A system configuration method for switching electrical power to each  
2 device interface circuit within a plurality of device interface circuits, wherein each  
3 said device interface circuit conditions signals transmitted between a  
4 microprocessor and a port connector electrically connected to said device  
5 interface circuit, and wherein said system configuration method comprises:

6 for each said device interface circuit, setting a bit position associated with  
7 said device interface circuit in a first register to a first state in response to  
8 electrically grounding a connection-sensing terminal within said port connector  
9 connected to said device interface circuit and to a second state in response to  
10 electrically floating said connection-sensing terminal; and

11 for each device interface circuit within said plurality of device interface  
12 circuits, performing a port configuration method including:

13 reading said bit position associated with said device interface circuit  
14 within said first register;  
15 reading a bit position associated with said device interface circuit  
16 within a second register;  
17 setting a bit position associated with said device interface circuit in  
18 said second register to a third state in response to determining that said  
19 bit position associated with said device interface circuit in said first register  
20 is in said first state and that said bit position associated with said device  
21 interface circuit in said second register is in a fourth state;  
22 setting said bit position associated with said device interface circuit  
23 in said second register to said fourth state in response to determining that  
24 said bit position associated with said device interface circuit in said first  
25 register is in said second state and that said bit position associated with  
26 said device circuit in said second register is in said third state;  
27 turning a switching device on to conduct electrical power to said  
28 device interface circuit in response to setting said bit position associated  
29 with said device interface circuit in said second register to said third state;  
30 and  
31 turning said switching device off in response to setting said bit p  
32 position associated with said device interface circuit in said second  
33 register to said fourth state.

1 19. The method of claim 18, wherein said port configuration method  
2 additionally includes:

3 loading a device driver routine used during operation of said device  
4 interface circuit in response to determining that said bit position associated with  
5 said device interface circuit in said first register is in said first state and that said  
6 bit position associated with said device interface circuit in said second register is  
7 in said fourth state; and



8 unloading a device driver routine used during operation of said device  
9 interface circuit in response to determining that said bit position associated with  
10 said device interface circuit in said first register is in said second state and that  
11 said bit position associated with said device circuit in said second register is in  
12 said third state.

1 20. The system configuration method of claim 18, additionally comprising:

2 following a first step attempting to write data through a device interface  
3 circuit in said plurality of device interface circuits, performing a system pausing  
4 method comprising:

5 reading a bit position set to indicate whether electrical power is  
6 supplied to said device interface circuit;

7 in response to determining that electrical power is not supplied to  
8 said device interface circuit, displaying a message indicating a cable is not  
9 attached to said port connector electrically connected to said device  
10 interface circuit and providing a graphical user interface allowing a user  
11 selection to continue after connecting a cable to said port connector; and

12 in response to receiving an input from said graphical user interface,  
13 again attempting to write data through said device interface circuit; and

14 following a first step attempting to read data through a device interface  
15 circuit in said plurality of device interface circuits, performing a system pausing  
16 method comprising:

17 reading a bit position set to indicate whether electrical power is  
18 supplied to said device interface circuit;

19 in response to determining that electrical power is not supplied to  
20 said device interface circuit, displaying a message indicating a cable is not  
21 attached to said port connector electrically connected to said device  
22 interface circuit and providing a graphical user interface allowing a user  
23 selection to continue after connecting a cable to said port connector; and

24 in response to receiving an input from said graphical user interface,  
25 again attempting to read data through said device interface circuit.

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